CLAIMS

1. An integrated circuit comprising:

a counter operative to receive an input clock signal with a first frequency, an M value and an N value, where the M value and the N value are each integer values, and to generate a counter signal having a second frequency determined by the M value and the N value; and

a delay generator operative to receive the counter signal and an L-bit control signal, where L is an integer greater than one, to generate a differential signal based on the counter signal and the L-bit control signal, and to use the differential signal to provide an output clock signal having the second frequency, wherein leading edges of the output clock signal are variably delayed in accordance with the L-bit control signal.

2. The integrated circuit of claim 1, wherein the delay generator includes:

a first bank of capacitors, each capacitor in the first bank being selectable by the L-bit control signal,

a first current source operative to charge selected capacitors in the first bank, and

a comparator operative to provide the output clock signal based on a first voltage signal on the selected capacitors in the first bank.

3. The integrated circuit of claim 2, wherein the delay generator further includes:

a second bank of capacitors, each capacitor in the second bank being selectable by the L-bit control signal; and

a second current source operative to discharge selected capacitors in the second bank, and wherein the differential signal is defined by the first voltage signal on the selected capacitors in the first bank and a second voltage signal on the selected capacitors in the second bank.

4. The integrated circuit of claim 3, wherein the delay generator further includes:

a first switch operative to discharge the capacitors in the first bank to a low voltage; and a second switch operative to precharge the capacitors in the second bank to a high voltage.

5. The integrated circuit of claim 2, wherein the first bank of capacitors is implemented with thermal decoding, and wherein the capacitors in the first bank have the same capacitance.

6. The integrated circuit of claim 2, wherein the first bank of capacitors is implemented with binary decoding, and wherein the first bank includes L capacitors having binary weighted capacitance.

7. The integrated circuit of claim 1, further comprising:

a current generator operative to provide a reference current for the delay generator, and wherein the variable delay for the leading edges of the output clock signal is obtained based on the reference current.

8. The integrated circuit of claim 7, wherein the current generator is implemented with a current locked loop.

9. The integrated circuit of claim 7, wherein the current generator includes:

a divider unit operative to divide the input clock signal in frequency to obtain a divided clock signal;

a replica delay generator operative to delay a first version of the divided clock signal by an adjustable delay and to provide a delayed clock signal;

a phase-frequency detector operative to compare phase of a second version of the divided clock signal against phase of the delayed clock signal and to provide a phase error;

a loop filter operative to filter the phase error and to provide a voltage signal; and

a converter operative to generate the reference current based on the voltage signal.

10. The integrated circuit of claim 9, wherein the divider unit is operative to divide the input clock signal by two in frequency, and wherein the replica delay

generator is operative to delay the first version of the divided clock signal by one half period of the input clock signal.

11. The integrated circuit of claim 7, wherein the current generator includes a replica delay generator operative to provide a predetermined amount of delay with the reference current.

12. The integrated circuit of claim 11, wherein the delay generator includes a first bank of capacitors and the replica delay generator includes a second bank of capacitors, wherein the capacitors in the first bank are matched to the capacitors in the second bank, and wherein the first and second banks of capacitors are arranged in a two-dimensional array.

13. The integrated circuit of claim 7, wherein the current generator is enabled prior to each leading edge of the output clock signal to generate the reference current for the delay generator and then disabled after each leading edge.

14. The integrated circuit of claim 1, further comprising:

a multiplier operative to receive and multiply an accumulator value from the counter with a Q value, where Q is an inverse of the M value and is used to generate the L-bit control signal.

15. The integrated circuit of claim 14, wherein the multiplier is implemented with a plurality of pipelined stages.

16. The integrated circuit of claim 14, wherein the multiplier is operative to perform rounding for the least significant bits (LSB) of the L-bit control signal.

17. The integrated circuit of claim 1, wherein the counter is operative to perform accumulation of the M value using a modulo-N accumulator for each cycle of the input clock signal.

18. The integrated circuit of claim 1, wherein the counter includes:

a first carry-save adder operative to add the M value with an accumulator value and to provide a first combined value;

a second carry-save adder operative to subtract the N value from the first combined value and to provide a second combined value and the counter signal, wherein the counter signal includes a pulse whenever an overflow occurs due to the first combined value being greater than or equal to the N value;

a multiplexer operative to provide the second combined value if overflow occurs and to provide the first combined value if overflow does not occur; and

a register operative to store the first or second combined value from the multiplexer and to provide the accumulator value.

19. The integrated circuit of claim 1, further comprising:

a dither generator operative to provide a dither signal, and wherein the counter is further operative to combine the dither signal with the M value and the N value to generate the counter signal.

20. The integrated circuit of claim 19, wherein the dither generator is implemented with a linear feedback shift register (LFSR), and wherein the dither signal is implemented to add zero frequency offset to the second frequency.

21. A device in a communication system, comprising:

a counter operative to receive an input clock signal with a first frequency, an M value, and an N value, where the M value and the N value are integer values, and to generate a counter signal having a second frequency determined by the M value and the N value; and

a delay generator operative to receive the counter signal and an L-bit control signal, where L is an integer value greater than one, to generate a differential signal based on the counter signal and the L-bit control signal, and to use the differential signal to provide an output clock signal having the second frequency, wherein leading edges of the output clock signal are variably delayed in accordance with the L-bit control signal.

22. The device of claim 21, wherein the delay generator includes:

a bank of capacitors implemented with thermal decoding, each capacitor in the bank being selectable by the L-bit control signal and having a unit capacitance;

a current source operative to charge selected capacitors in the bank; and

a comparator operative to provide the output clock signal based on a voltage signal on the selected capacitors in the bank.

23. The device of claim 21, further comprising:

a current generator operative to provide a reference current for the delay generator, and wherein the variable delay for the leading edges of the output clock signal is obtained based on the reference current.

24. The device of claim 23, wherein the current generator implements a current locked loop and includes a replica delay generator operative to provide a predetermined amount of delay with the reference current.

25. The device of claim 21, further comprising:

a multiplier operative to receive and multiply an accumulator value from the counter with a Q value, where the Q value is an inverse of the M value and is used to generate the L-bit control signal.

26. The device of claim 21, wherein the communication system is a Code Division Multiple Access (CDMA) communication system.

27. An apparatus comprising:

means for receiving an input clock signal with a first frequency, an M value and an N value, where the M value and the N value are each integer valued;

means for generating a counter signal with the input clock signal and the M value and the N value, wherein the counter signal has a second frequency determined by the M value and the N value;

means for generating a differential signal based on the counter signal and an L-bit control signal, where L is an integer greater than one;

means for comparing the differential signal; and

means for providing, based on the comparing, an output clock signal having the second frequency, wherein leading edges of the output clock signal have variable delay determined by the L-bit control signal.

28. The apparatus of claim 27, further comprising:

means for charging selected ones of capacitors in a first bank; and

means for discharging selected ones of capacitors in a second bank, and wherein the differential signal is defined by a first voltage signal on selected capacitors in the first bank and a second voltage signal on selected capacitors in the second bank.

29. The apparatus of claim 27, further comprising:

means for generating a reference current used to obtain the variable delay for the leading edges of the output clock signal.

30. The apparatus of claim 29, further comprising:

means for generating a predetermined amount of delay, and wherein the reference current is generated to obtain the predetermined amount of delay.

31. The apparatus of claim 27, further comprising:

means for generating an accumulator value with the M and N values and the input clock signal; and

means for multiplying the accumulator value with a Q value, where Q is an inverse of M, to provide the L-bit control signal.